AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

1-10. (Canceled)

11. (Currently Amended) A design support apparatus for supporting wiring design for bond wires that connect a semiconductor chip and an interposer, the design support apparatus comprising:

an input control unit receiving input data including ~~at least~~ dimensions of a semiconductor chip and an interposer, and bond wire coordinate information containing arrangement positions of bond wires for connecting the semiconductor chip to the interposer;

a creating unit that creates simulated design data that simulates, based on the input data, an occurrence of deviation in an arrangement position of the semiconductor chip on the interposer and an occurrence of deviation in bond wire connection terminal positions of the interposer based on the arrangement positions of the bond wires contained in the input data and the simulated deviation in the arrangement position of the semiconductor chip on the interposer, wherein the creating unit creates the simulated design data prior to arrangement of the semiconductor chip on the interposer; and

an analyzing unit that analyzes, based on the simulated design data, deficiencies in manufacturing of semiconductor devices due to the deviation in the

arrangement position of the semiconductor chip on the interposer and the deviation in the bond wire connection terminal positions of the interposer, and outputs analysis results that are used to design a semiconductor package based on the input data and the manufacturing deficiencies.

12. (Currently Amended) A design support apparatus for supporting wiring design for bond wires that connect a semiconductor chip and an interposer, the design support apparatus comprising:

an input control unit receiving input data including ~~at least~~ dimensions of a semiconductor chip and an interposer, and bond wire coordinate information containing arrangement positions of bond wires for connecting the semiconductor chip to the interposer;

a creating unit that creates simulated design data that simulates, based on the input data, an occurrence of deviation in an arrangement position of the semiconductor chip on the interposer and an occurrence of deviation in bond wire connection terminal positions of the interposer based on the arrangement positions of the bond wires contained in the input data and the simulated deviation in the arrangement position of the semiconductor chip on the interposer, wherein the creating unit creates the simulated design data prior to arrangement of the semiconductor chip on the interposer; and

an analyzing unit that analyzes, based on the simulated design data, a tolerance of the deviation in the arrangement position of the semiconductor chip on the interposer and a tolerance of the deviation in the bond wire connection terminal

positions of the interposer, and outputs analysis results that are used to design a semiconductor package based on the input data and the tolerances.

13. (Currently Amended) A design support apparatus for semiconductor devices comprising:

an input control unit receiving input design data including ~~at least~~ dimensions of a semiconductor chip and an interposer, and bond wire coordinate information containing arrangement positions of bond wires for connecting the semiconductor chip to the interposer;

a first data creating unit that creates, based on the input design data of the semiconductor package, semiconductor chip simulated arrangement data obtained by arranging the semiconductor chip in a position where deviation in an arrangement position of the semiconductor chip on the interposer is simulated such that an arrangement position of the semiconductor chip is simulated to deviate ~~the deviation of the semiconductor chip~~ from an original position ~~is simulated~~included in the input design data;

a second data creating unit that creates, based on the design data of the semiconductor package and the simulated deviation in the arrangement position of the semiconductor chip on the interposer contained in the semiconductor chip simulated arrangement data, bond wire simulation data obtained by wiring, using bond wires, the bond wire connection terminals of the semiconductor chip arranged to deviate from ~~an~~ the arrangement positions of the bond wires in the design data and bond wire connection terminals of the interposer, wherein the second data

creating unit creates the bond wire simulation data prior to arrangement of the semiconductor chip on the interposer;

a measuring unit that measures a design rule for the bond wires used for the wiring from the bond wire simulation data; and

an analyzing unit that analyzes measurement results obtained by the measuring unit, and outputs analysis results that are used to design the semiconductor package based on the bond wire simulation data and the measurement results.

14. (Currently Amended) The design support apparatus according to claim 13, wherein the design data of the semiconductor package further includes a shape of the interposer, a shape of the semiconductor chip, an arrangement position of the semiconductor chip on the interposer, and a shape of the bond wires that connect the semiconductor chip and the interposer., ~~and arrangement positions of the bond wires that connect the semiconductor chip and the interposer.~~

15. (Previously Presented) The design support apparatus according to claim 13, wherein the first data creating unit creates semiconductor chip simulated arrangement data obtained by arranging, with respect to the arrangement position of the semiconductor chip on the interposer in the design data of the semiconductor package, the semiconductor chip in a position where fluctuation in deviation of an arrangement position of the semiconductor chip in an in-plane direction or a rotation direction on a semiconductor chip arrangement surface of the interposer or

fluctuation deviation in inclination of the semiconductor chip in a thickness direction of the interposer is simulated.

16. (Previously Presented) The design support apparatus according to claim 13, wherein the measuring unit measures clearance between the bond wires and clearance between the bond wires and the semiconductor chip as the design rule.

17. (Previously Presented) The design support apparatus according to claim 16, wherein the analyzing unit analyzes a tolerance of fluctuation in the deviation of an arrangement position of the semiconductor chip on the interposer that satisfies the design rule.

18. (Previously Presented) The design support apparatus according to claim 16, wherein the analyzing unit analyzes a tolerance of fluctuation in the deviation of the bond wire connection terminal positions of the interposer that satisfies the design rule.

19. (Previously Presented) The design support apparatus according to claim 13, comprising a storing unit that stores therein the measurement result.

20. (Currently Amended) The design support apparatus according to claim 13, comprising a storing unit that stores therein an analysis result obtained by the analyzing unit.

21. (New) The design support apparatus according to claim 11, wherein the creating unit creates the simulated design data prior to connection of bond wires to at least one of the semiconductor chip and the interposer.

22. (New) The design support apparatus according to claim 11, wherein the input data includes an arrangement position of the semiconductor chip on the interposer, and the creating unit creates the occurrence of deviation in the arrangement position of the semiconductor chip on the interposer based on the arrangement position of the semiconductor chip on the interposer included in the input data.

23. (New) The design support apparatus according to claim 12, wherein the creating unit creates the simulated design data prior to connection of bond wires to at least one of the semiconductor chip and the interposer.

24. (New) The design support apparatus according to claim 12, wherein the input data includes an arrangement position of the semiconductor chip on the interposer, and the creating unit creates the occurrence of deviation in the arrangement position of the semiconductor chip on the interposer based on the arrangement position of the semiconductor chip on the interposer included in the input data.

25. (New) The design support apparatus according to claim 13, wherein the second data creating unit creates the bond wire simulation data prior to connection of bond wires to at least one of the semiconductor chip and the interposer.

26. (New) The design support apparatus according to claim 13, wherein the input design data includes an arrangement position of the semiconductor chip on the interposer, and the second data creating unit creates the semiconductor chip simulated arrangement data based on the arrangement position of the semiconductor chip on the interposer included in the input design data.